IN THE SPECIFICATION:

Page 1, before paragraph [0001], insert the following heading and paragraph:

Cross Reference to Related Application(s)

The subject matter of this application is related to application Serial No. _____ (attorney docket No. T2147-908626), filed concurrently herewith in the name of Andrzej WOZNIAK, entitled « Procédé et système d'établissement automatique d'un modèle global de simulation d'une architecture » (English title: « System and Method for Automatically Generating a Global Simulation Model of An Architecture ", and corresponding to French Application No. FR 02/09690 filed July 30, 2002, the subject matter of which is hereby incorporated by reference.--

Page 1, please substitute the following paragraphs [0001] and [0002]:

Field of the Invention

[0001] The invention concerns a method and a system for the automatic recognition of simulation configurations for the functional verification of ASIC integrated circuits through simulation tests. More specifically, the invention concerns a method for automatic recognition of simulation configurations and a system for implementing the method.

Background of the Invention

[0002] With the increase in the complexity of hardware systems, it is necessary to be able to deal with system configurations that are increasingly combining models written in a hardware description language, for example of the HDL type (the languages VDHL and Verilog being the most frequently used), and in high level languages of the HLL type (such as C or C++); these languages describe both the elements constituting the hardware and the models constituting the simulation environment.

Please substitute paragraph [0007] as follows:

Summary of the Invention

[0007] ~~The~~ One object of the present invention is to limit the drawbacks of test program debugging based on available simulation configurations.

Please substitute paragraphs [0017] and [0018] as follows:

Brief Description of the Drawings

[0017] The invention will be better understood with the help of the following description of an exemplary embodiment of the method of the invention, in reference to the attached drawings, in which:

- Fig. 1 represents, in a very schematic form, an exemplary global simulation model ;

- Fig. 2 represents a diagram illustrating the various components of the automatic recognition system and the steps for implementing these components in the method of the invention;

- Figs. 3a through 3c represent various stages in the modeling of a circuit using a mixed model of the HDL (VERILOG or VDHL) type and the HLL (C++) type~~.~~ and

- Figs. 4a through 4c represent various configurations of the global simulation model corresponding to the architecture represented in Fig. 1.

Description of the Preferred Embodiments

[0018] A global simulation model is typically composed of one or more models of integrated circuits being tested (DUTs) surrounded by models that create a test and verification environment. These models create complex stimuli and receive complex responses from the model tested. These components can be transactors (XACTORS) – models generally having a program interface (API) that allows control by tests outside the model, these tests generally being written in high level language (HLL).